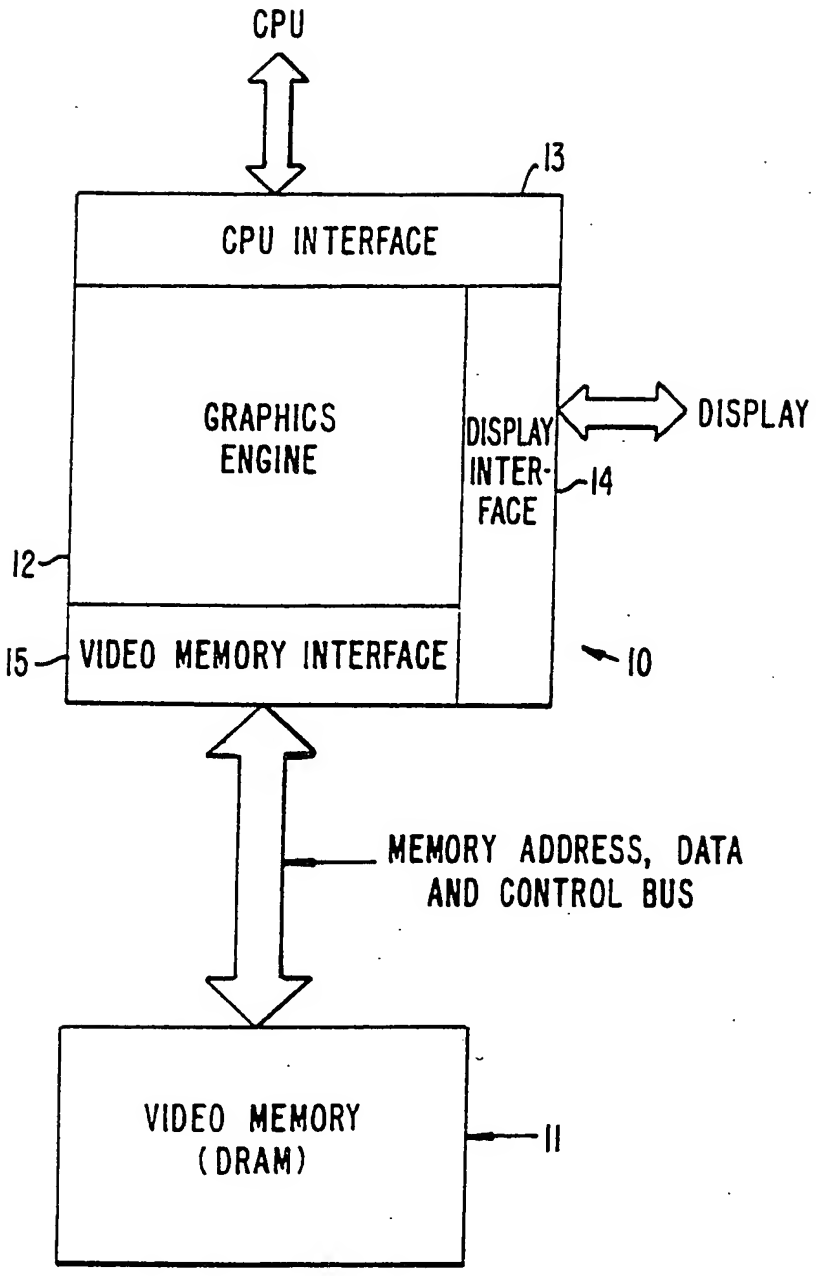

FIG. 1.

PRIOR ART

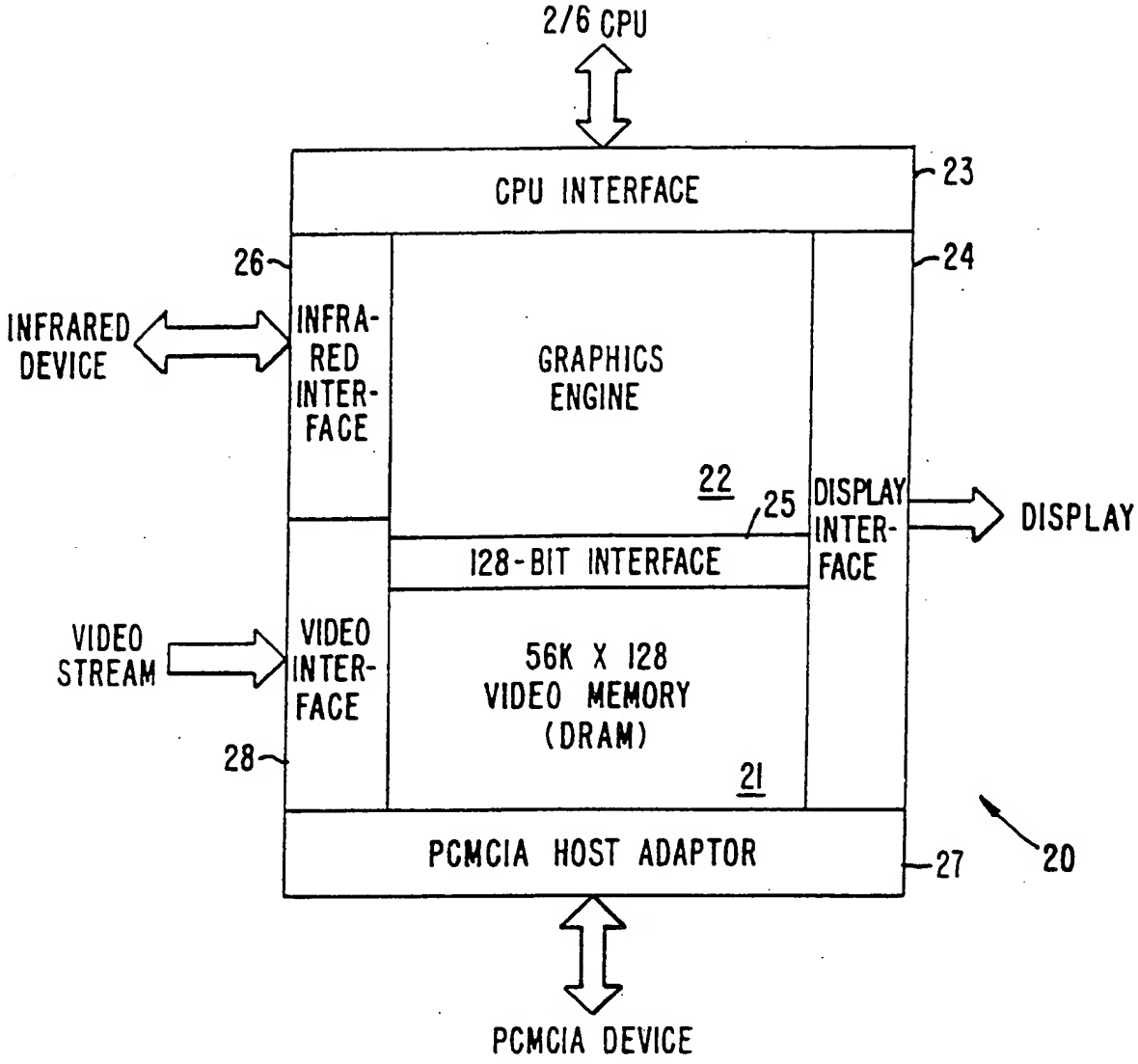

FIG. 2.

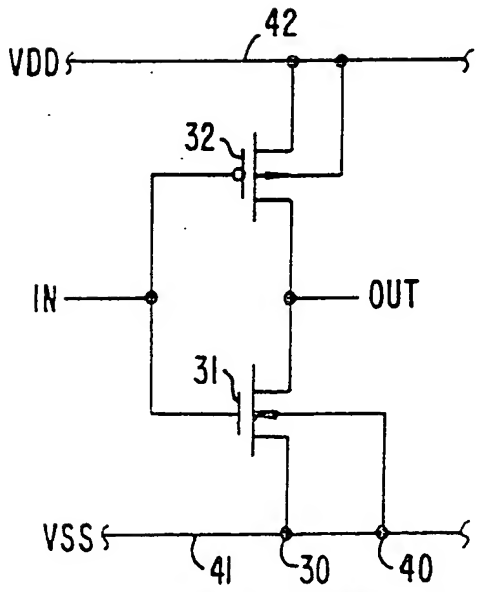

FIG. 3A.

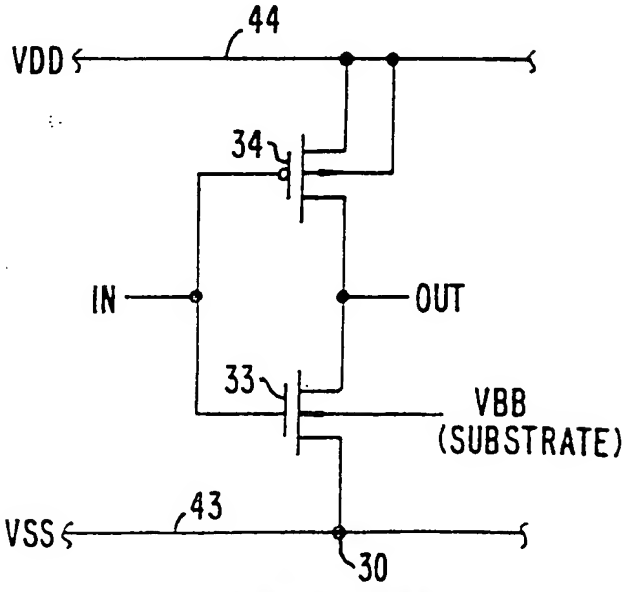

FIG. 3B.

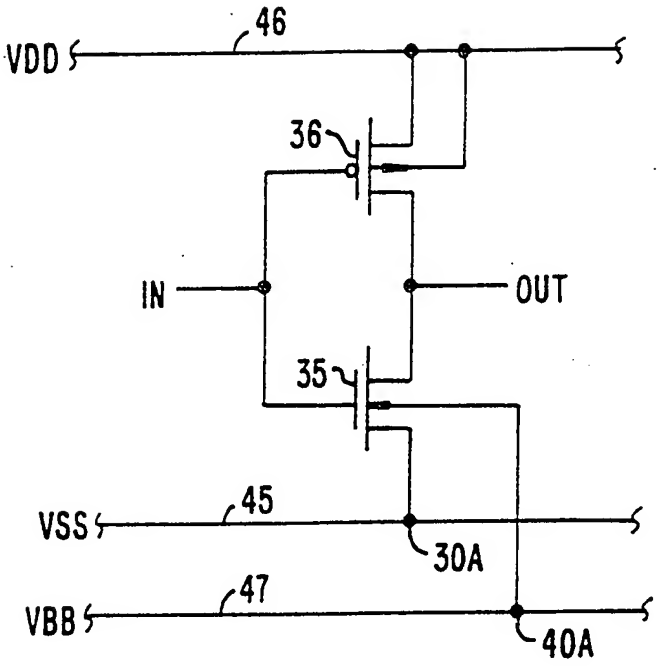
VDD
46
36
IN
OUT
35
VSS
45
30A
VBB
47
40A

FIG. 4.

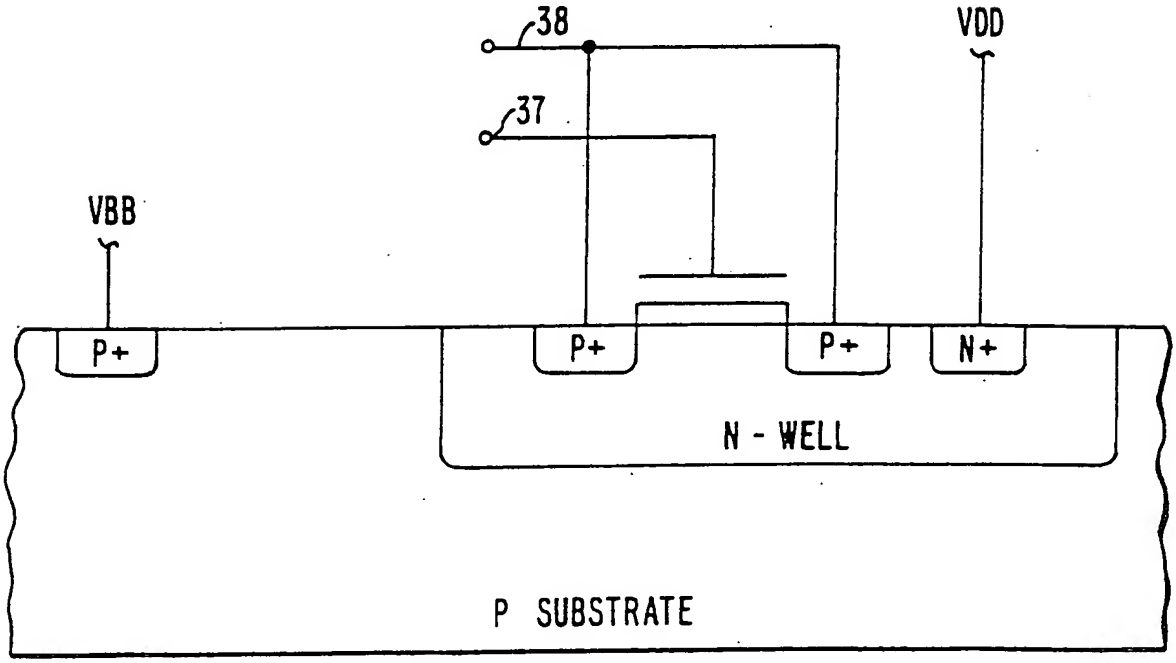
38
37
VDD
VBB
P+
P+
P+
N+
N - WELL
P SUBSTRATE

FIG. 5.

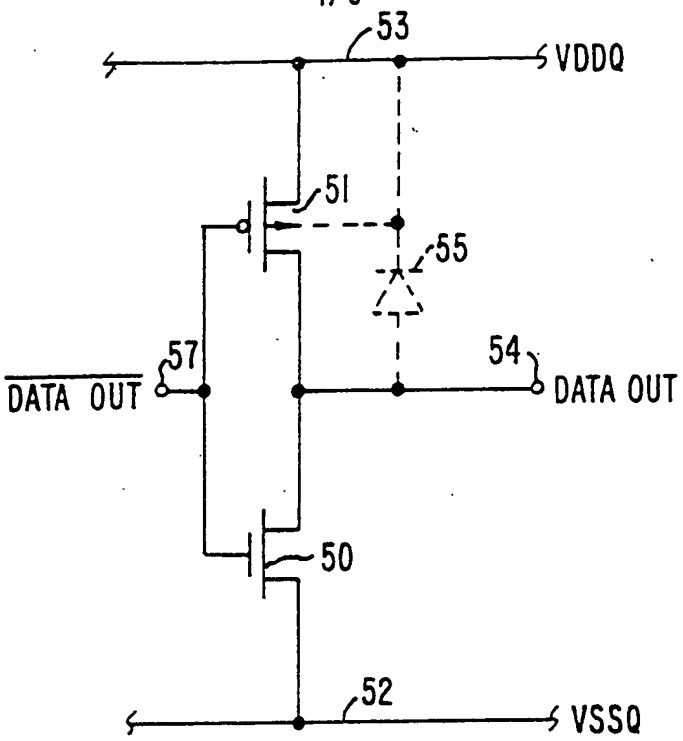

FIG. 6A.
PRIOR ART

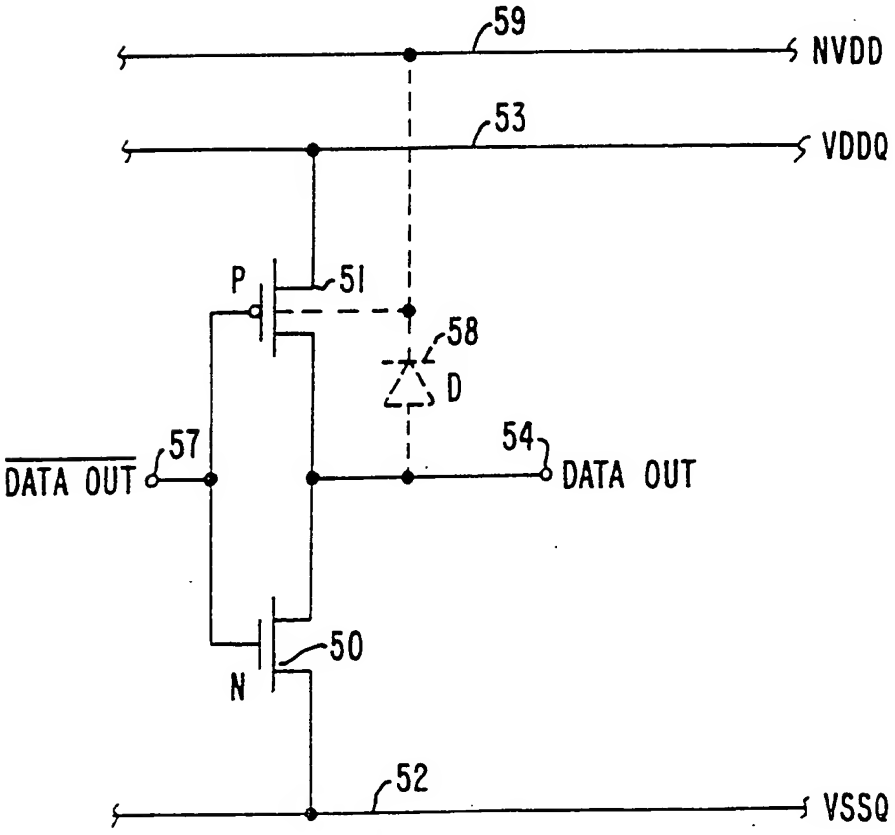

FIG. 6B.

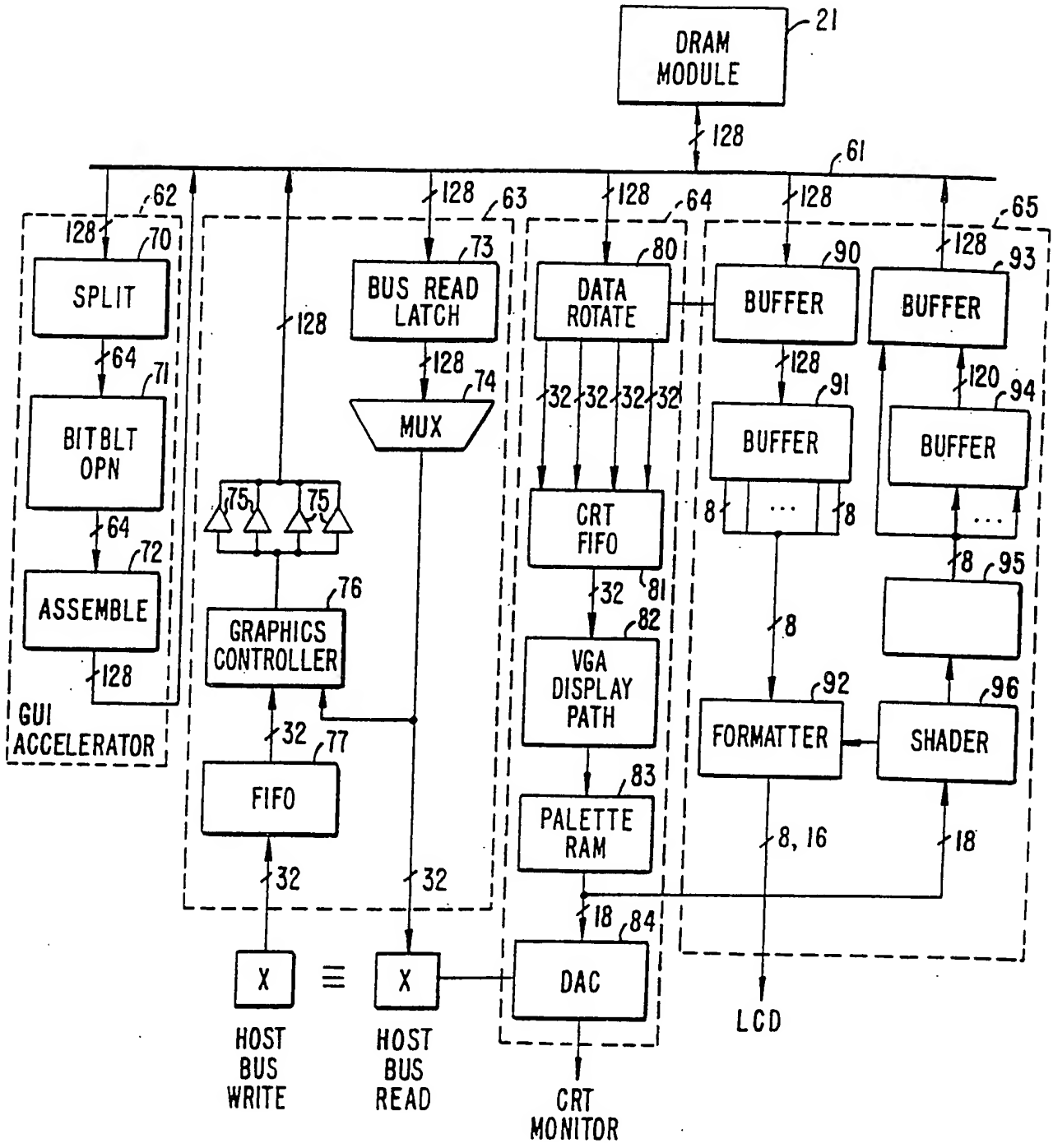
DRAM MODULE
21
128
61
62
63
64
65
128
SPLIT
70
64
BITBLT OPN
71
64
ASSEMBLE
72
128
GUI ACCELERATOR
128
BUS READ LATCH
73
128
MUX
74
75
75
GRAPHICS CONTROLLER
76
32
FIFO
77
32
32
X
≡
X
HOST BUS WRITE
HOST BUS READ
DATA ROTATE
80
32 32 32 32
CRT FIFO
81
32
VGA DISPLAY PATH
82
PALETTE RAM
83
18
84
DAC
CRT MONITOR
BUFFER
90
128
BUFFER
91
8 ... 8
8
FORMATTER
92
8, 16
LCD
128
93
BUFFER
120
94
BUFFER
... 8
95
96
SHADER
18

FIG. 7.

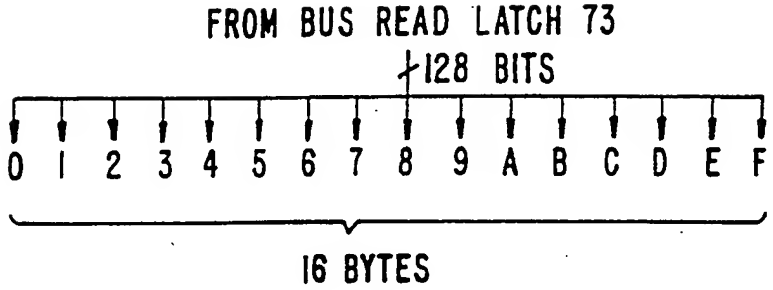

FIG. 8.

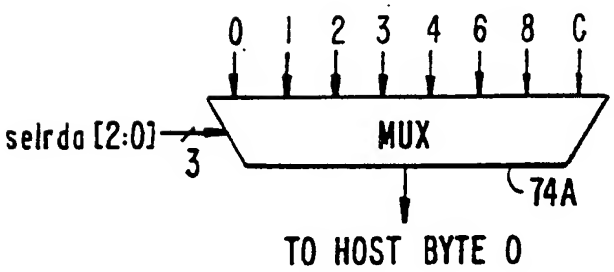

FIG. 9A.

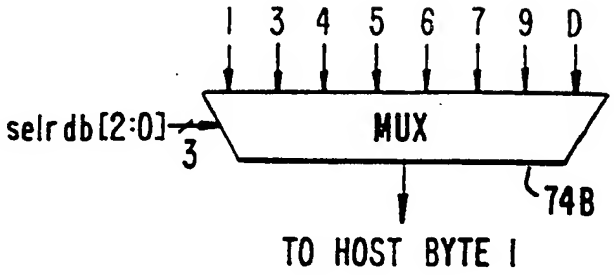

FIG. 9B.

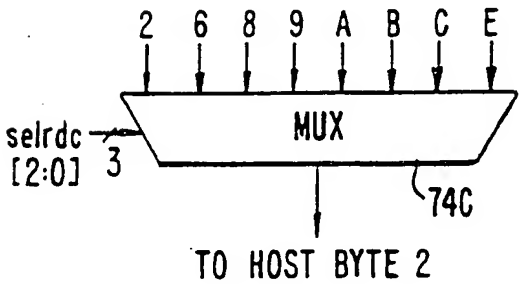

FIG. 9C.

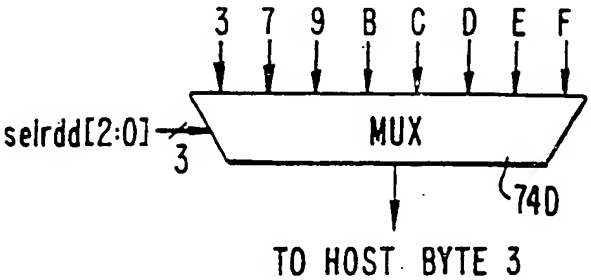

FIG. 9D.